IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A parallel pseudo-random binary sequence checker comprising:

a receiving means for receiving a pseudo-random binary sequence ~~in parallel n-bit sample~~, wherein said pseudo-random binary sequence is generated by a pseudo-random binary sequence generator n bits at a time in parallel;

means for automatically synchronizing the state of said receiving means with an n-bit sample within said pseudo-random binary sequence to ~~provide~~ generate a next n-bit sample within said pseudo-random binary sequence; ~~and~~

means for comparing said next generated n-bit sample within said pseudo-random binary sequence to ~~said~~ a corresponding next received n-bit sample within said pseudo-random binary sequence~~, wherein said comparing means indicates~~; and

means for indicating an error condition has occurred if said next generated n-bit sample within said pseudo-random binary sequence does not equal to said corresponding next received n-bit sample within said pseudo-random binary sequence.

2. (currently amended) The checker of Claim 1, wherein said checker further includes ~~a plurality of latches and a plurality of XOR gates connected to a subset of said plurality of latches;~~

means for loading 16 most significant bits to said checker;

means for loading 15 least significant bits to said checker; and

means for serially advancing ~~said~~ a plurality of latches within said checker twice.

3. (currently amended) The checker of Claim 1, wherein said checker further includes a multiplexor within said pseudo-random binary sequence generator for yielding output bits in parallel.

4. (currently amended) The checker of Claim 1, wherein said checker further includes a mask register for masking specific bits in error.

5. (currently amended) The checker of Claim 1, wherein said checker further includes ~~an error window start register and an error window end register coupled to~~ an error counter for counting a number of errors occurred since said checker was reset.

6. (currently amended) The checker of Claim 1, wherein said checker further includes ~~a sync detect start register, a sync detect end register, a sync detect threshold register and~~ a sync detector to indicate an occurrence of a failed synchronization.

7. (currently amended) A method for synchronizing a parallel pseudo-random binary sequence checker, said method comprising:

receiving a pseudo-random binary sequence ~~in parallel n-bit sample~~ by a receiving means, wherein said pseudo-random binary sequence is generated by a pseudo-random binary sequence generator n bits at a time in parallel;

automatically synchronizing the state of said receiving means with an n-bit sample within said pseudo-random binary sequence to ~~provide~~ generate a next n-bit sample within said pseudo-random binary sequence; ~~and~~

comparing said next generated n-bit sample within said pseudo-random binary sequence to ~~said~~ a corresponding next received n-bit sample within said pseudo-random binary sequence~~, wherein said comparing means indicates~~; and

indicating an error condition has occurred if said next generated n-bit sample within said pseudo-random binary sequence does not equal to said corresponding next received n-bit sample within said pseudo-random binary sequence.

8. (currently amended) The method of Claim 7, wherein said method further includes

loading 16 most significant bits to said parallel pseudo-random binary sequence checker;

loading 15 least significant bits to said parallel pseudo-random binary sequence checker; and

serially advancing ~~said~~ a plurality of latches within said parallel pseudo-random binary sequence checker twice.

9. (currently amended) The method of Claim 7, wherein said method further includes providing a multiplexor within said pseudo-random binary sequence generator for yielding output bits in parallel.

10. (currently amended) The method of Claim ~~1~~ 7, wherein said method further includes providing a mask register for masking specific bits in error.

11. (currently amended) The method of Claim ~~1~~ 7, wherein said method further includes providing an error counter to count a number of errors occurred since said parallel pseudo-random binary sequence checker was previously reset.

12. (currently amended) The method of Claim ~~1~~ 7, wherein said method further includes providing a logical indication of an occurrent of a failed synchronization.